## REMARKS

Reconsideration of the above-identified application in view of the foregoing amendments and following remarks is respectfully requested.

### Status of the Claims

Claims 1-3, 5-6 and 9-19 are pending in this application, of which claims 14-19 are withdrawn, i.e., claims 1-3, 5-6 and 9-13 remain under consideration. Claims 1-3, 5-6 and 9-13 stand rejected. By this amendment, claims 1 and 5 are amended. Support for these claim amendments may be found throughout the application as originally filed including, e.g., paragraphs [0058]-[0072] and Figs. 6-7.

No new matter will be introduced into this application by entry of these amendments.

### Rejections under 35 U.S.C. § 102(b)

In paragraph two (2) of the Office Action, claims 1-3, 5-6 and 9-13 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent Appl. No. 2003/0102497 to Fried, et al. ("Fried").

Referring to Figs. 6 and 7 of the present application as reproduced below, the MIS transistor of claim 1 comprises, *inter alia*, a semiconductor substrate (702) that again comprises a projecting part (704) formed directly from the surface of the semiconductor substrate, and a gate insulator (708) formed on the surface of the semiconductor substrate including the projecting part, i.e., the region surrounded by a bold and broken lines that define the channel of the transistor. In particular claim 1 recites that at least one of the top surface and a side wall of the projecting part has a secondary crystal plane (e.g., 110) different from the principal crystal plane (e.g., 100). With the features of the invention as discussed herein, the channel of the transistor

can be formed along the sidewalls of the projecting part thereby extending the channel width of the transistor by the two times of the height of the sidewalls (i.e., both sides of the projecting part). See, e.g., paragraph [0084] of the corresponding published application (i.e., U.S. Pub. No. 2006/0278909 A1).

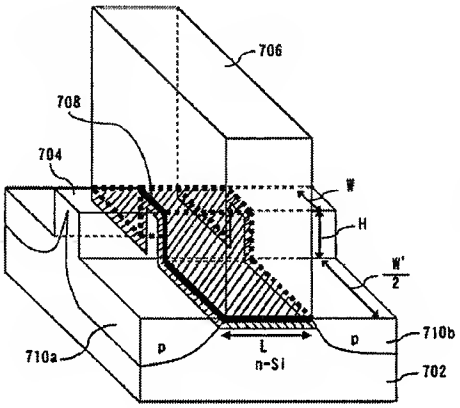


FIG. 6

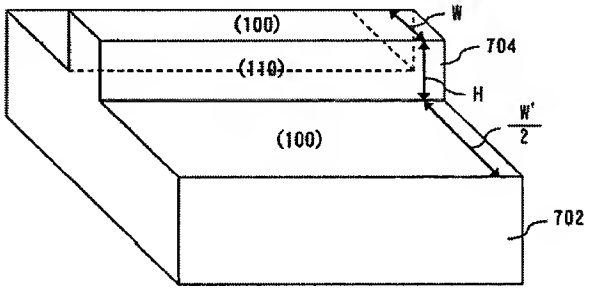


FIG. 7

Fried discloses a CMOS device structure in which multiple FinFETs (i.e., a double gated FET) are formed on the same substrate. Referring to Figs. 7a and 7b as shown below, Fried device comprises two separate gated transistors (i.e., a left side device and a right side device) formed side by side on the same substrate 204 which is an insulating layer of a SOI wafer.

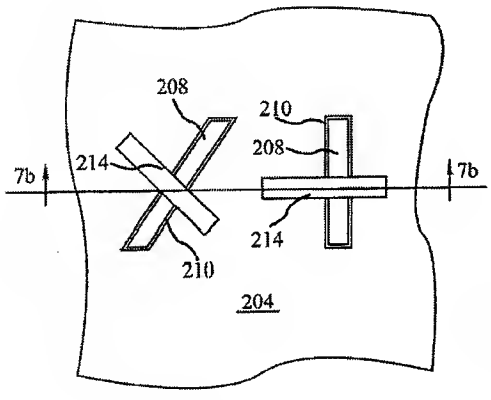


FIG. 7a

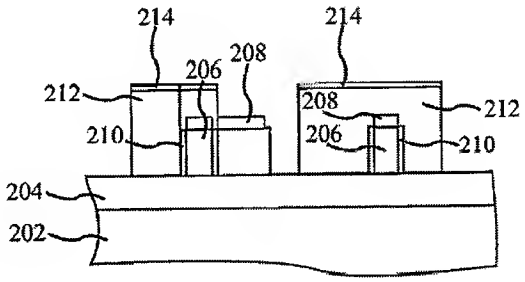


FIG. 7b

Fried reveals that the FinFET comprises, *inter alia*, a semiconductor layer (206) and gate insulator (210) formed by, e.g., a thermal oxidation of the semiconductor layer. The FinFET structure also includes a gate conductor layer (212), and a hard mask film (208, 214).

However, Applicants believe that Fried does not disclose each and every element of claim 1. For example, while claim 1 recites "a semiconductor substrate" having a projecting part formed directly from the surface of the semiconductor substrate, Fried's projecting part (i.e., the semiconductor layer 206 as asserted by the Examiner[1]) is not formed directly from a surface of the semiconductor substrate. Rather, Fried's projecting part 206 is formed from a separate layer of the buried insulator layer 204. As a result, Fried further fails to teach the "gate insulator" of claim 1 that is formed on the semiconductor substrate including the projecting part.

Moreover, the Examiner indicated that:

> A gate insulator (208 & 210) formed on the semiconductor substrate including the projecting part in such a way that the gate insulator covers at least a portion of the semiconductor substrate, the top surface and the sidewall of the projecting part (first of all, 208 & 210 directly touch all of the above, including 204 which would be 202 in non-SOI embodiment, as was made clear above, and thus meets the limitations. Furthermore, this is not shown in FIG. 7b since it is a SOI embodiment, but, the 210 or another oxide would ***inherently*** be under the entire gate 212, ***otherwise*** the gate would short to the semiconductor substrate and the device would not operate; this is an ***inherent*** feature; for the purpose of demonstrating a point, and not prior art, see FIG. 8 of US-5391509 by Tada; gate insulator 30 is everywhere under the gate electrode 32; again, this is an inherent feature of MIS/MOS transistors).[2] [Emphasis in the original]

First of all, Applicants note that the Fried's insulator 208 is not a gate insulator that will form a real channel of a transistor but is "a hard mask film" utilized as a mask (e.g., an etch stop) to pattern the semiconductor layer (206) underneath. See, e.g., paragraph [0046] of Fried. Also, Applicants believe that the Examiner is making an improper proposition without a reference that a non-SOI embodiment would be assumed to meet the claim limitations. However, As Applicants explained above, since one of the purposes of the projecting part of claim 1 is to

[1] Page 3 of the Office Action.

[2] Page 3 of the Office Action.

extend the channel width, it is important that this projecting part is formed directly from the surface of the same semiconductor substrate. Otherwise, the channel may be discontinued and the transistor may not be operated as intended.

Secondly, while Applicants understand that an insulating layer (e.g., the gate insulator 210) is normally provided between a gate electrode (e.g., the gate conductor layer 212) and a semiconductor layer (e.g., the semiconductor layer 206) to form a channel region of the transistor, Applicants' clam 1 is not directed to this aspect. Rather, claim 1 recites "a gate insulator" formed on the semiconductor substrate including the projecting part that, again, is formed directly from the surface of the semiconductor substrate.

In view of the above, Applicants believe that claim 1 is neither anticipated by nor rendered obvious in view of the reference cited by the Examiner (i.e., Fried) for at least the reasons discussed above.

Nonetheless, claims 1 and 5 have been amended for further clarification. In particular, each of amended claims 1 and 5 recites, *inter alia*, that "a plurality of channel regions formed at said top surface of said projecting part, at the surface of said side wall of said projecting part and at the surface of said at least a portion of said semiconductor substrate, all under said gate insulator." This element of amended claims 1 and 5 makes it clear that a channel is formed not only at the normal surface of the semiconductor substrate but also at the projecting part of the semiconductor surface all under the gate insulator.

Applicants believe that amended claims 1 and 5 further distinguish over the reference cited by the Examiner, Fried. Reconsideration and withdrawal of the rejections of claims 1 and 5 under 35 U.S.C. § 102(b) is respectfully requested.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Furthermore, Applicants have not specifically addressed the rejections of the dependent claims. Applicants respectfully submit that the independent claims, from which they depend, are in condition for allowance as set forth above. Accordingly, the dependent claims also are in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

Applicants believe that this application as amended is in condition for allowance and such action is respectfully requested.

## CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is earnestly solicited. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 50-4827, ORDER NO. 1004378.52910.

Respectfully submitted,
Locke Lord Bissell & Liddell LLP

Dated: April 27, 2009

By: Steven F. Meyer
Steven F. Meyer
Registration No. 35,613

Correspondence Address:
Locke Lord Bissell & Liddell LLP
3 World Financial Center
New York, NY 10281-2101
(212) 415-8600 Telephone
(212) 303-2754 Facsimile